



Doc Code: AP.PRE.REQ

PTO/SB/SS (07-05)

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

000174-0195-102

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on March 28, 2007

Signature

Rose Marie Dhanraj

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ROSE MARIE DHANRAJ

Application Number

10/781,051

Filed

February 17, 2004

First Named Inventor

Edward Flaherty

Art Unit

2825

Examiner

Naum B. Levin

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.

See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

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Registration number 26,183

☐ attorney or agent acting under 37 CFR 1.34.

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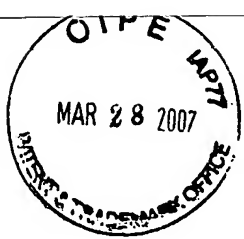
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

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CONCISE ARGUMENT FOR WHICH REVIEW IS BEING REQUESTED

I. Introduction

Claims 1-40 are pending in this patent application. Of these, claims 6-8 and 26-34 have been withdrawn from consideration due to a restriction requirement. Claims 1-5, 9-25, and 35-40 remain under consideration. The independent claims that remain under consideration are 1, 9, 17, and 35.

All of the claims remaining under consideration have been finally rejected under 35 U.S.C. § 102 as anticipated by Narasimhan et al. U.S. patent 6,446,192 ("Narasimhan").

In the case of each of applicants' claims, the Examiner has omitted one or more essential elements needed for a prima facie rejection. This will be shown in detail in the following sections of this Request.

II. Claims 1-5

Claim 1 specifies a method of configuring an integrated circuit ("IC") chip that includes programmable logic circuitry. This method includes programming the programmable logic circuitry to function as communications port circuitry, using that programmed circuitry to make a connection to an off-chip source of more programming data, bringing in that additional programming data, and then using that additional data "to reprogram said programmable logic circuitry to function as other than communications port circuitry." (Emphasis added.) Thus, in accordance with claim 1, programmable logic circuitry on an IC is first used as what may be called a "soft" communications port, via which additional programming data is brought into the chip. Then that additional programming data is used to convert the programmable logic of the soft port to something completely different, which is not a communications port at all. In the words of applicants' specification (e.g., page 13, lines 10-11), this reprogramming "typically

wipes out the preliminary configuration of PLD 40 as a communications port.” (Emphasis added.) Nothing like this is shown in Narasimhan.

It appears to the signer of this Request that all of the various communications ports in Narasimhan are dedicated circuitry to at least some extent. Some of these ports may be “programmable” in some respects. But the signer of this Request sees no clear teaching that programmable logic circuitry employed in these ports can be put to some other, non-communications-port-circuitry use (as is required by the last element of applicants’ claim 1). (The preceding sentence assumes, without conceding, that there is programmable logic circuitry associated with one or more communications ports in Narasimhan.)

The portion of the final rejection that purports to demonstrate that the last element of claim 1 can be found in Narasimhan (i.e., the first full paragraph on page 4 of the January 3, 2007 final rejection) does not in fact do that. The first quotation in that paragraph is from applicants’ specification, not from Narasimhan. The subsequent underscored paraphrasings from Narasimhan seem to the signer of this Request to have nothing to do with reconfiguring an initial programmable logic circuitry communications port to another non-communications-port function. For example, what does the final rejection’s general assertion about “a versatile collection of layered protocols” have to do with the last element of applicants’ claim 1? Similarly, what relevance to this claim element have the final rejection’s assertions about “a security sockets layer,” “security functionality,” “a secure sockets layer,” “transport layer security,” “network interface ... security,” or “a password”? The signer of this Request can see no relevance of any of these alleged aspects of Narasimhan to the specifics of claim 1. The Examiner has therefore not met his burden of establishing a prima facie case that claim 1 is

anticipated by Narasimhan. Claim 1 and its dependent claims 2-5 should accordingly be allowed.

III. Claim 9-16

Claim 9 specifies, inter alia, that an Ethernet MAC connection is made; that data comes into the chip via that connection; that the connection is then severed; and that the data that was brought into the chip is used to program programmable logic of the chip for operations subsequent to severing of the connection.

In contrast to all of this detail in claim 9, the Examiner can only point to Narasimhan's ability to "refuse" a connection that is not supported by a correct password. Thus, for example, the portion of page 5 of the January 3, 2007 final rejection that purports to deal with the latter portion of claim 5 paraphrases Narasimhan as providing "login authentication," in which, "upon connection, the user is prompted for a password [and] if the password is not correct, the connection will be refused." Even assuming that "refused" means that the connection is actually broken (i.e., severed, as specified by applicants in claim 9), this feature of Narasimhan does not teach what applicants specify in claim 9 (i.e., making an Ethernet MAC connection, bringing data in via that connection, severing the connection, and then using the data that was brought in to program the chip for operations subsequent to severing the connection).

Once again, the Examiner has not met his burden of showing, prima facie, that Narasimhan anticipates claim 9. Claim 9 and its dependent claims 10-16 should therefore be allowed.

IV. Claims 17-25

Claim 17 specifies establishing a meaningful connection via Ethernet MAC circuitry, bringing data into the chip via that connection for use in programming programmable

logic circuitry on the chip, and then severing the Ethernet MAC connection. Once again, the only thing the January 3, 2007 final rejection cites to anticipate this is Narasimhan's ability to "refuse" a connection that is not supported by a correct password. This prior art citation does not include at least the element of claim 17 that the Ethernet MAC connection is used to bring into the chip data for programming programmable logic of the chip prior to severing the Ethernet MAC connection. Omission of at least this claim element from the prior art citation means that the Examiner has again failed to make a prima facie rejection of claim 17. Claim 17 and its dependent claims 18-25 should accordingly be allowed.

V. Claims 35-40

Claim 35 is another claim that specifies, inter alia, making a meaningful Ethernet MAC connection, bringing programming data into the chip via that connection, and then severing the Ethernet MAC connection. Once again, the final rejection cites only the "refused" connection feature of Narasimhan as anticipating these requirements of claim 35. This prior art does not in fact anticipate all of the features of claim 35. Indeed, it is really irrelevant to the point of claim 35. Because the above-mentioned elements of claim 35 are not all shown by Narasimhan, the Examiner has again failed to make a prima facie rejection of claim 35. Claim 35 and its dependent claims 36-40 should therefore be allowed.

VI. Conclusion

The foregoing demonstrates that claims 1-5, 9-25, and 35-40 are allowable. Panel review of the final rejection of these claims and prompt allowance of this application are accordingly respectfully requested.